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Double Data Rate (DDR3) SDRAM Controller IP Core User Guide IPUG80 Version 1.9, October 2016Documents. 0 download. Report. ... Local Interface of DDR3 Controller Core is implemented as a pipeline which enables the memory access request in each clock as long ...DDR3 CONTROLLER DESIGN DDR3 CONTROLLER DESIGN Pavan Kumar Reddy (621638) Brindha AG (621685) Vaishnavi S (621703) Lekshmi Vishwanath (621653) Amritha Krishna R S (621663)The Xilinx DDR3 core can generate a full controller or phy only for custom controller needs.